

**OptiMOS® Power-Transistor**

**Feature**

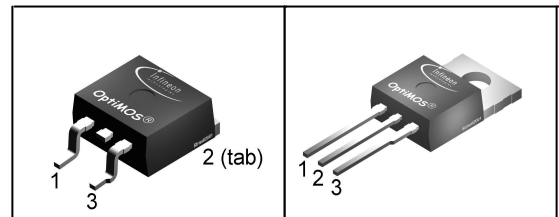
- N-Channel
- Enhancement mode
- Logic Level
- 175°C operating temperature
- Avalanche rated
- $dv/dt$  rated

**Product Summary**

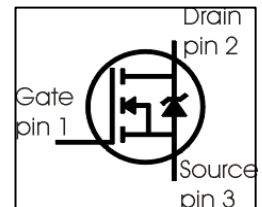
$V_{DS}$	75	V
$R_{DS(on)}$ max. SMD version	6.8	mΩ
$I_D$	80	A

P- TO263 -3-2

P- TO220 -3-1



Type	Package	Ordering Code	Marking
SPP80N08S2L-07	P- TO220 -3-1	Q67060-S6015	2N08L07
SPB80N08S2L-07	P- TO263 -3-2	Q67060-S6016	2N08L07



**Maximum Ratings, at  $T_j = 25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Value	Unit
Continuous drain current 1) $T_C=25\text{ °C}$	$I_D$	80 80	A
Pulsed drain current $T_C=25\text{ °C}$	$I_{D\text{ puls}}$	320	
Avalanche energy, single pulse $I_D=80\text{ A}$ , $V_{DD}=25\text{ V}$ , $R_{GS}=25\text{ Ω}$	$E_{AS}$	810	mJ
Repetitive avalanche energy, limited by $T_{jmax}^{2)}$	$E_{AR}$	30	
Reverse diode $dv/dt$ $I_S=80\text{ A}$ , $V_{DS}=60\text{ V}$ , $di/dt=200\text{ A/μs}$ , $T_{jmax}=175\text{ °C}$	$dv/dt$	6	kV/μs
Gate source voltage	$V_{GS}$	±20	V
Power dissipation $T_C=25\text{ °C}$	$P_{tot}$	300	W
Operating and storage temperature	$T_j, T_{stg}$	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	0.3	0.5	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	62	
SMD version, device on PCB: @ min. footprint @ 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	62 40	

**Electrical Characteristics, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	75	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=250\mu A$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=75V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=75V, V_{GS}=0V, T_j=125^\circ C^2)$	$I_{DSS}$	-	0.01 1	1 100	$\mu A$
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	$I_{GSS}$	-	1	100	nA
Drain-source on-state resistance $V_{GS}=4.5V, I_D=67A$ $V_{GS}=4.5V, I_D=67A, \text{SMD version}$	$R_{DS(on)}$	-	6.5 6.2	9 8.7	$m\Omega$
Drain-source on-state resistance 4) $V_{GS}=10V, I_D=67A$ $V_{GS}=10V, I_D=67A, \text{SMD version}$	$R_{DS(on)}$	-	5.3 5	7.1 6.8	

<sup>1</sup>Current limited by bondwire ; with an  $R_{thJC} = 0.5K/W$  the chip is able to carry  $I_D= 135A$  at  $25^\circ C$ , for detailed information see app.-note ANPS071E available at [www.infineon.com/optimos](http://www.infineon.com/optimos)

<sup>2</sup>Defined by design. Not subject to production test.

<sup>3</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu m$  thick) copper area for drain connection. PCB is vertical without blown air.

<sup>4</sup>Diagrams are related to straight lead versions

**Electrical Characteristics**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic Characteristics**

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 80A$	74	148	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0V$ , $V_{DS} = 25V$ , $f = 1MHz$	-	5130	6820	pF
Output capacitance	$C_{oss}$		-	993	1320	
Reverse transfer capacitance	$C_{rss}$		-	415	620	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 40V$ , $V_{GS} = 10V$ , $I_D = 80A$ , $R_G = 1.1\Omega$	-	25	38	ns
Rise time	$t_r$		-	81	122	
Turn-off delay time	$t_{d(off)}$		-	76	114	
Fall time	$t_f$		-	78	117	

**Gate Charge Characteristics**

Gate to source charge	$Q_{gs}$	$V_{DD} = 60V$ , $I_D = 80A$	-	18	23	nC
Gate to drain charge	$Q_{gd}$		-	66	83	
Gate charge total	$Q_g$	$V_{DD} = 60V$ , $I_D = 80A$ , $V_{GS} = 0$ to $10V$	-	186	233	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 60V$ , $I_D = 80A$	-	3.3	-	V

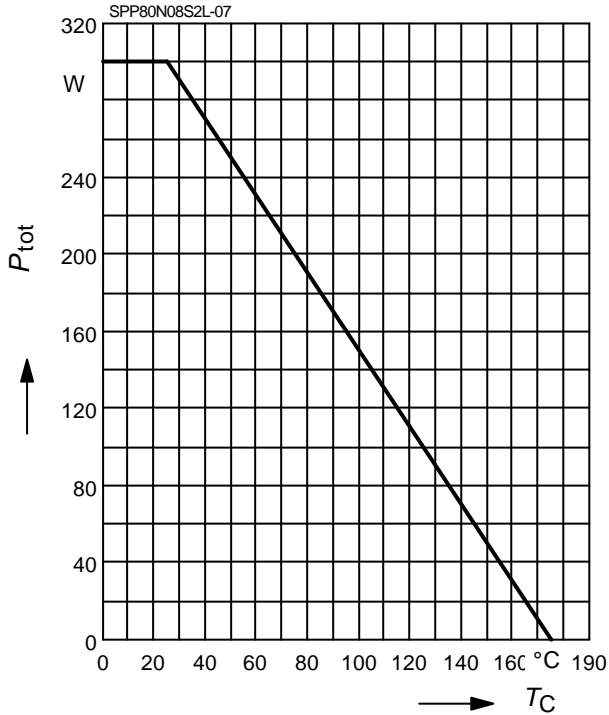
**Reverse Diode**

Inverse diode continuous forward current	$I_S$	$T_C = 25^\circ C$	-	-	80	A
Inv. diode direct current, pulsed	$I_{SM}$		-	-	320	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0V$ , $I_F = 80A$	-	0.9	1.3	V
Reverse recovery time	$t_{rr}$	$V_R = 40V$ , $I_F = I_S$ , $di_F/dt = 100A/\mu s$	-	81	100	ns
Reverse recovery charge	$Q_{rr}$		-	197	250	

### 1 Power dissipation

$$P_{tot} = f(T_C)$$

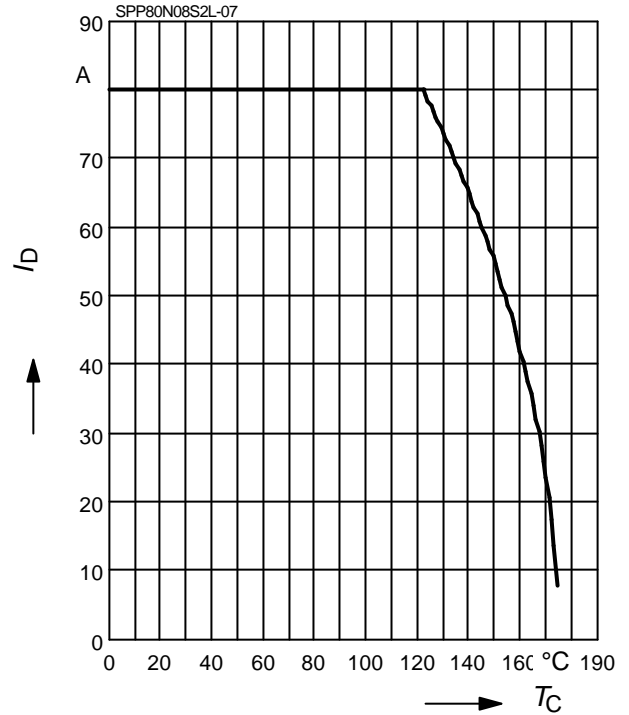
parameter:  $V_{GS} \geq 4 \text{ V}$



### 2 Drain current

$$I_D = f(T_C)$$

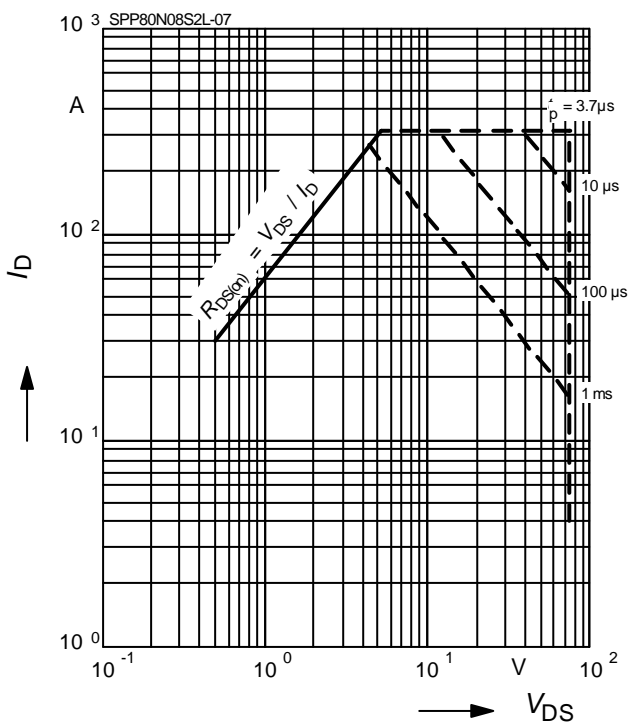
parameter:  $V_{GS} \geq 10 \text{ V}$



### 3 Safe operating area

$$I_D = f(V_{DS})$$

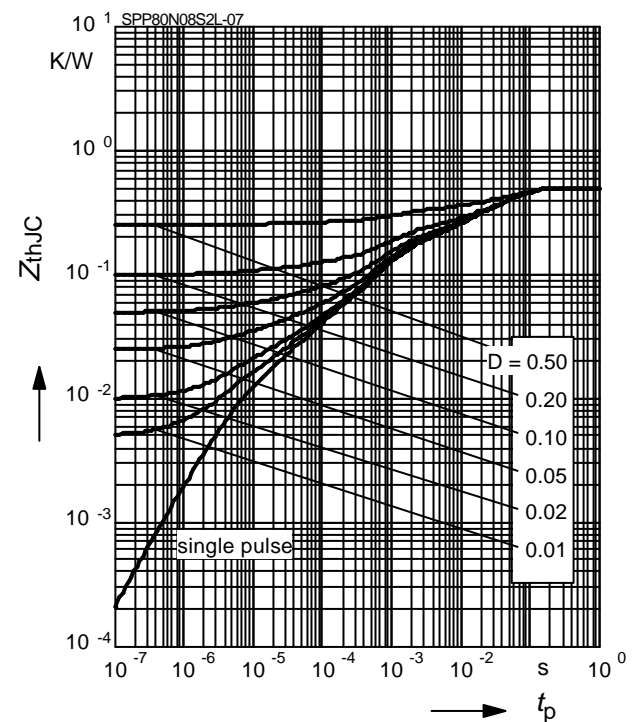
parameter:  $D = 0.01$ ,  $T_C = 25 \text{ °C}$



### 4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

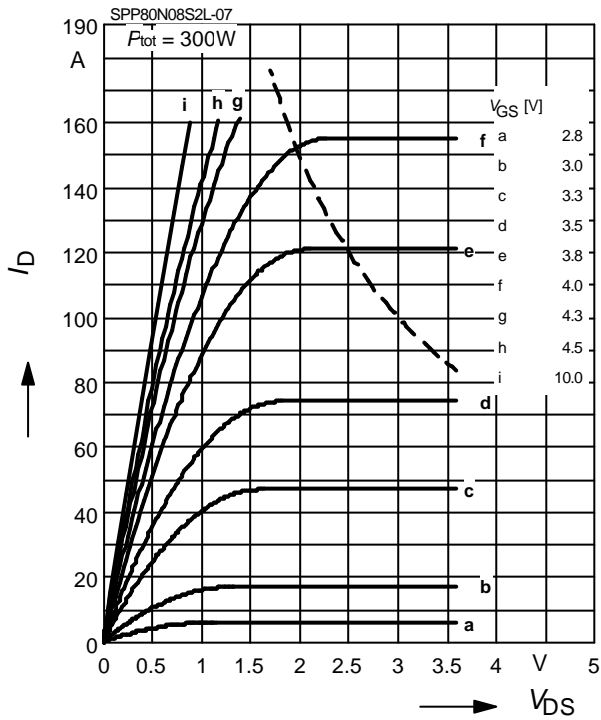
parameter:  $D = t_p/T$



**5 Typ. output characteristic**

$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$

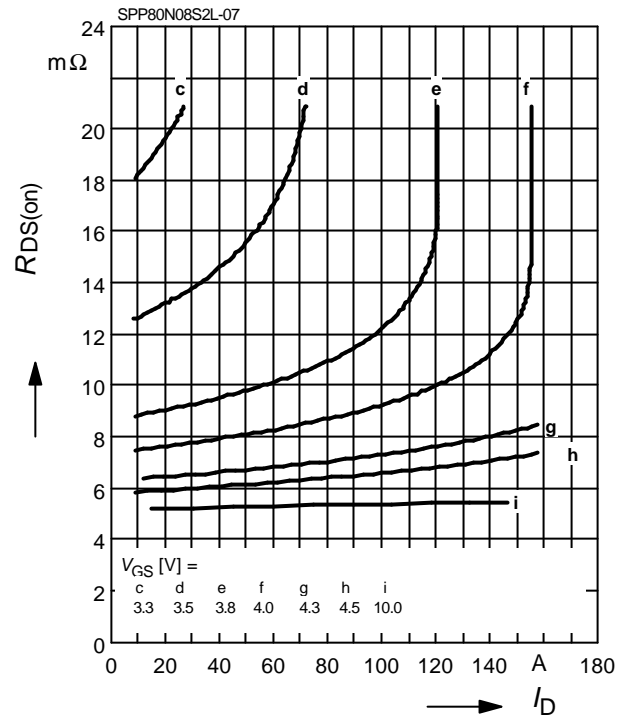
parameter:  $t_p = 80 \mu\text{s}$



**6 Typ. drain-source on resistance**

$R_{DS(\text{on})} = f(I_D)$

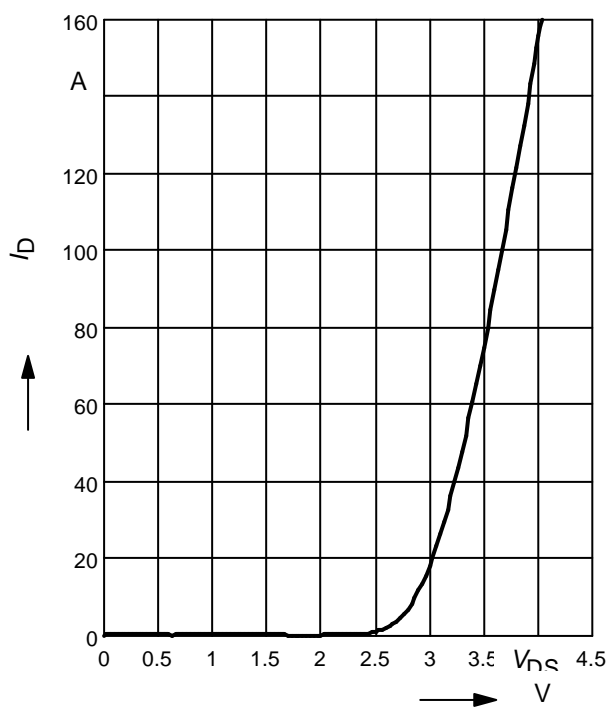
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(\text{on})\text{max}}$

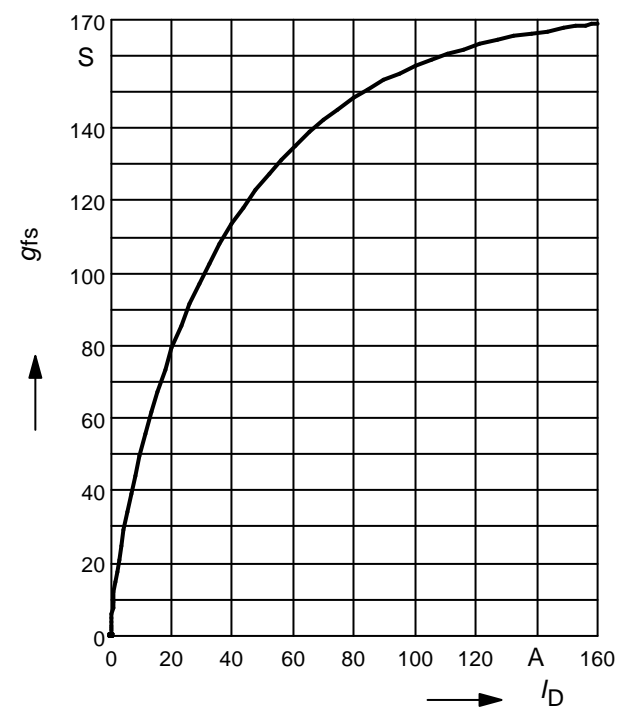
parameter:  $t_p = 80 \mu\text{s}$



**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_J = 25^\circ\text{C}$

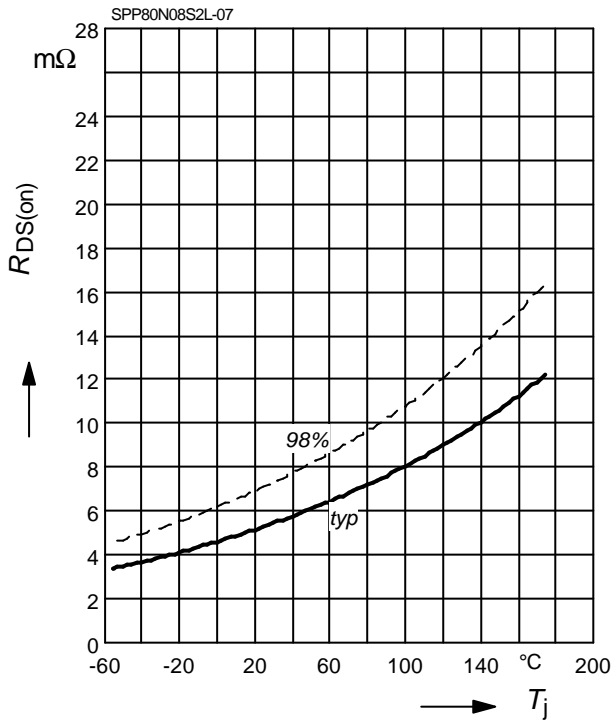
parameter:  $g_{fs}$



**9 Drain-source on-state resistance**

$$R_{DS(on)} = f(T_j)$$

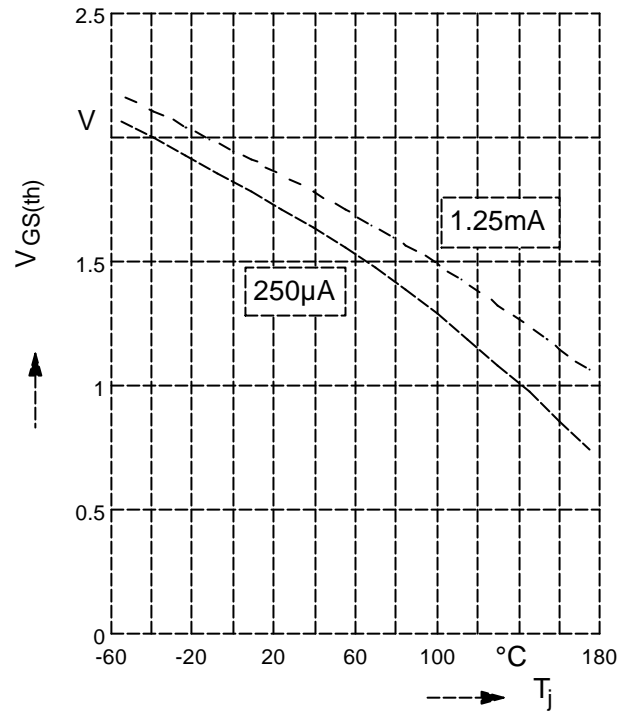
parameter :  $I_D = 67\text{ A}$ ,  $V_{GS} = 10\text{ V}$



**10 Typ. gate threshold voltage**

$$V_{GS(th)} = f(T_j)$$

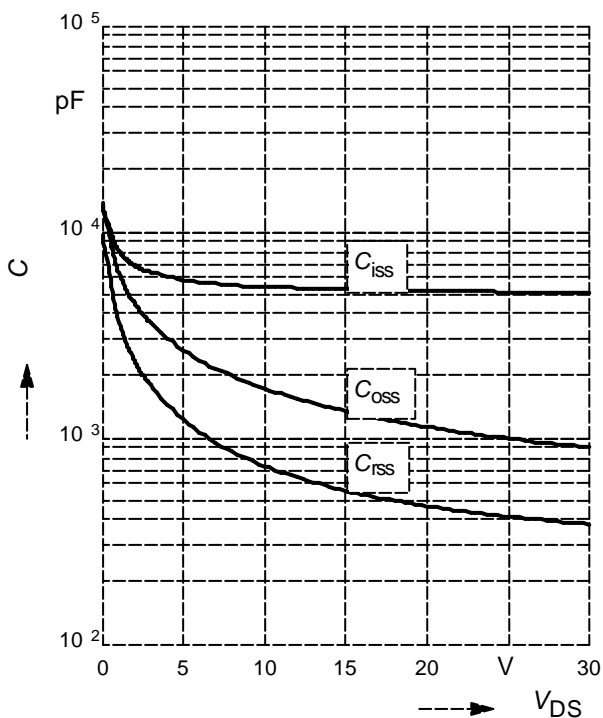
parameter:  $V_{GS} = V_{DS}$



**11 Typ. capacitances**

$$C = f(V_{DS})$$

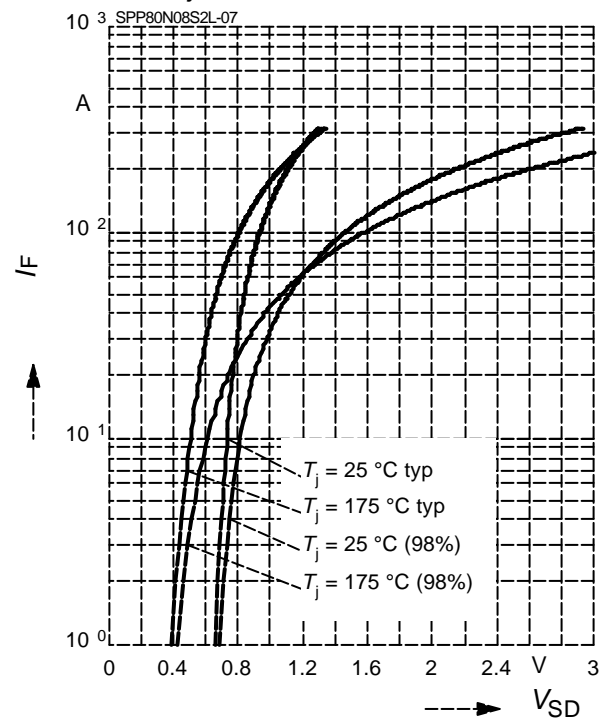
parameter:  $V_{GS}=0\text{V}$ ,  $f=1\text{ MHz}$



**12 Forward character. of reverse diode**

$$I_F = f(V_{SD})$$

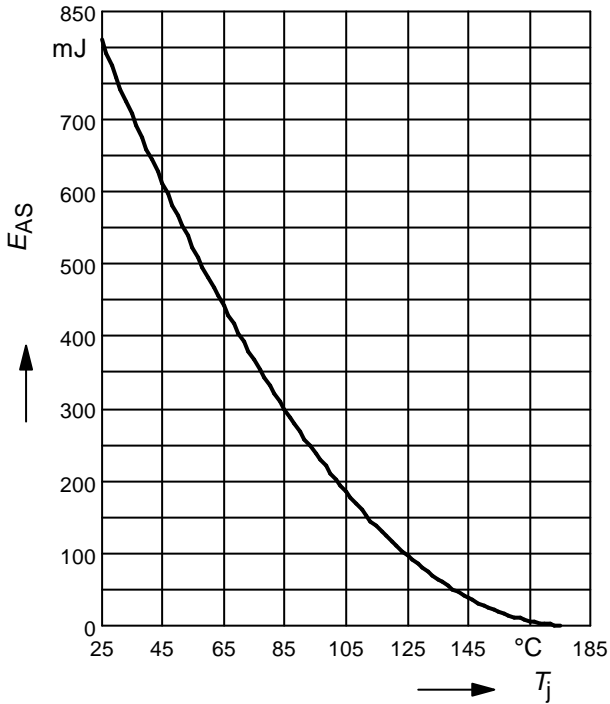
parameter:  $T_j$ ,  $t_p = 80\text{ μs}$



**13 Typ. avalanche energy**

$$E_{AS} = f(T_j)$$

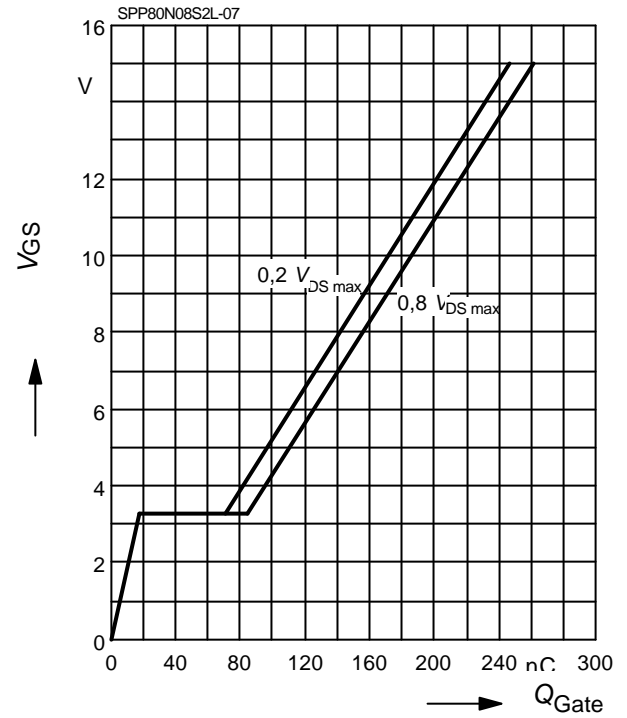
par.:  $I_D = 80 \text{ A}$  ,  $V_{DD} = 25 \text{ V}$  ,  $R_{GS} = 25 \Omega$



**14 Typ. gate charge**

$$V_{GS} = f(Q_{Gate})$$

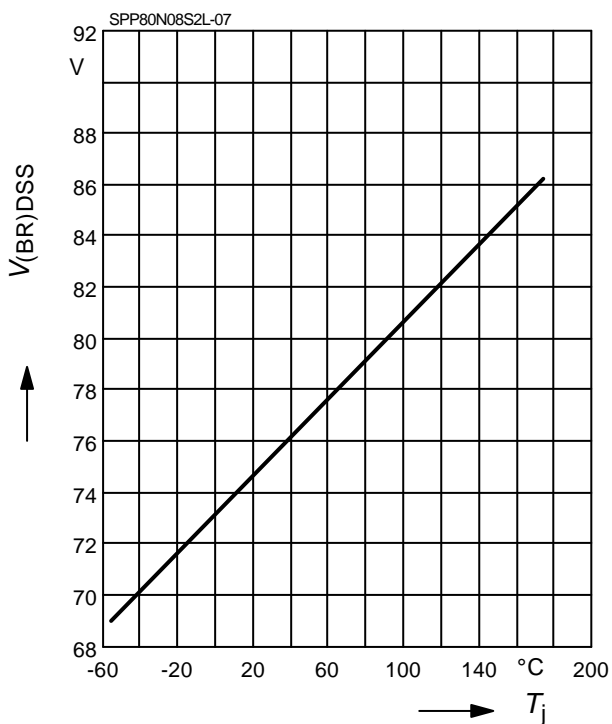
parameter:  $I_D = 80 \text{ A}$  pulsed



**15 Drain-source breakdown voltage**

$$V_{(BR)DSS} = f(T_j)$$

parameter:  $I_D = 10 \text{ mA}$



**Published by**  
**Infineon Technologies AG,**  
**Bereichs Kommunikation**  
**St.-Martin-Strasse 53,**  
**D-81541 München**  
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**Further information**

Please notice that the part number is **BSPP80N08S2L-07** and **BSPB80N08S2L-07**, for simplicity the device is referred to by the term **SPP80N08S2L-07** and **SPB80N08S2L-07** throughout this documentation.